Fig.1

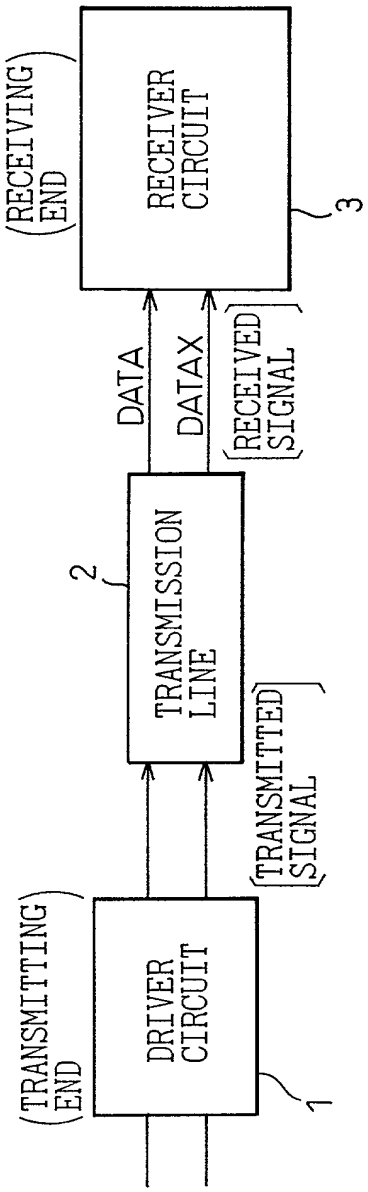

(TRANSMITTING END)
DRIVER CIRCUIT
1
(TRANSMITTED SIGNAL)
2
TRANSMISSION LINE
DATA
DATAX
(RECEIVED SIGNAL)
(RECEIVING END)
RECEIVER CIRCUIT
3

Fig.2

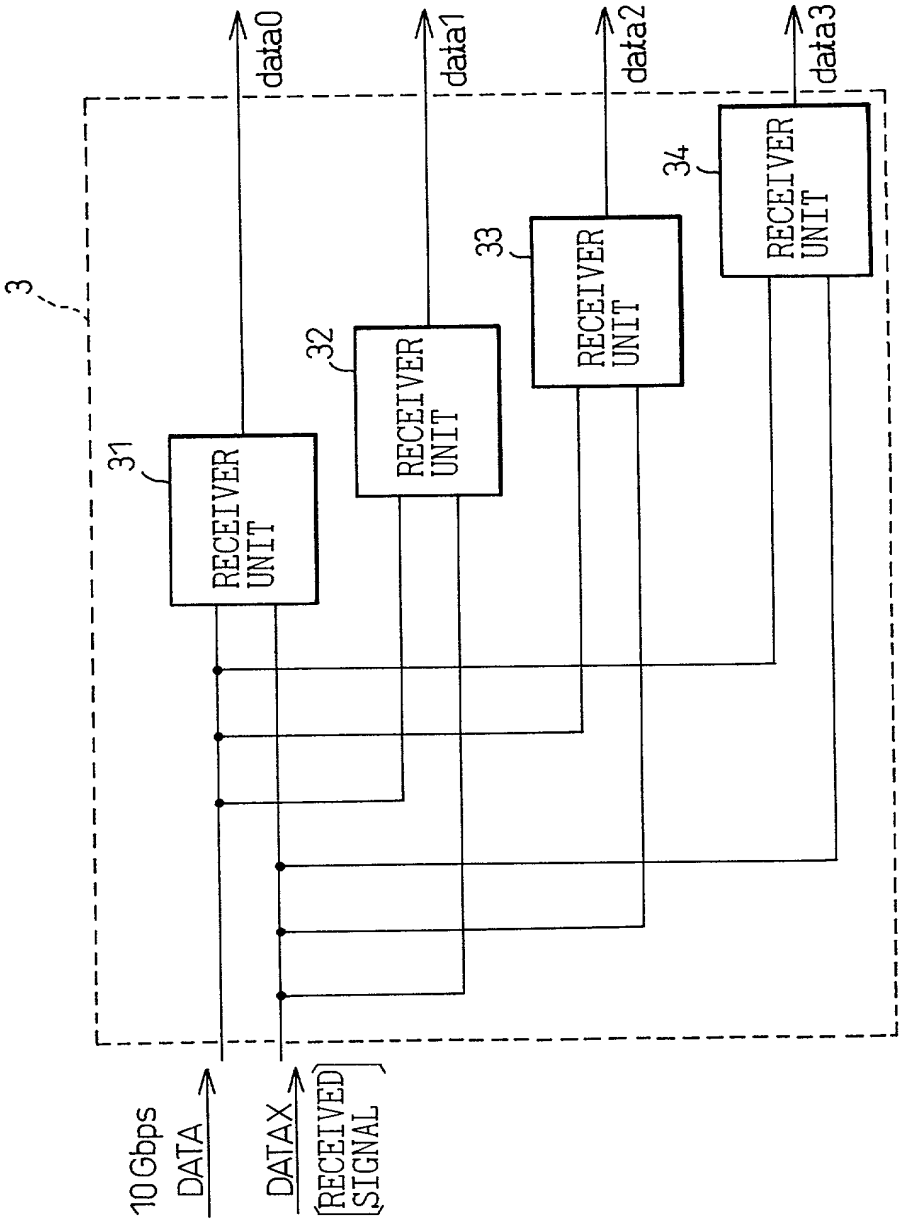

3
31
32
33
34
RECEIVER UNIT
RECEIVER UNIT
RECEIVER UNIT
RECEIVER UNIT
data0
data1
data2
data3
10Gbps DATA
DATAX (RECEIVED SIGNAL)

Fig.3

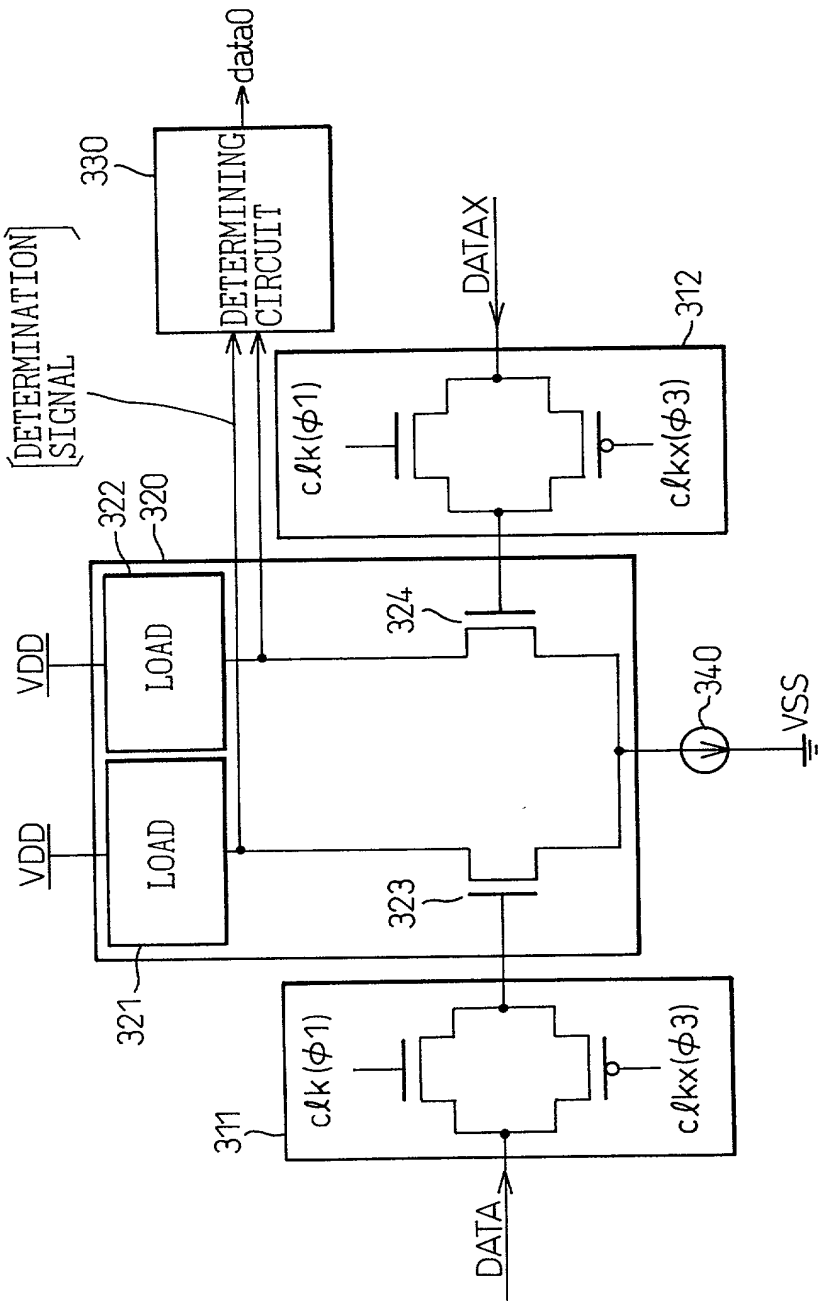

31
DETERMINATION SIGNAL
330
DETERMINING CIRCUIT
data0
DATAX
312
clk(φ1)
clkx(φ3)
322
320
VDD
LOAD
VDD
LOAD
324
323
340
VSS
321
311
clk(φ1)
clkx(φ3)
DATA

Fig.4A

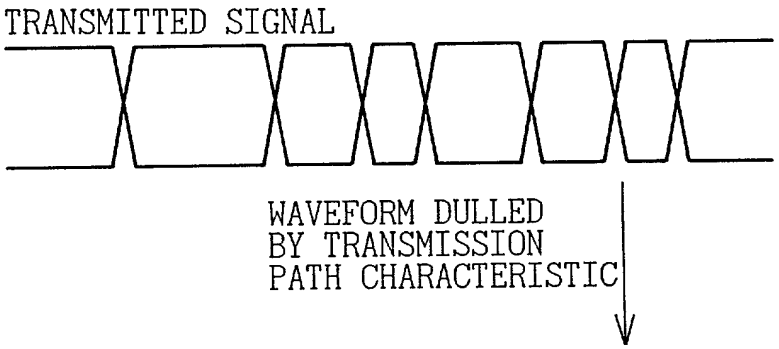


Fig.4B

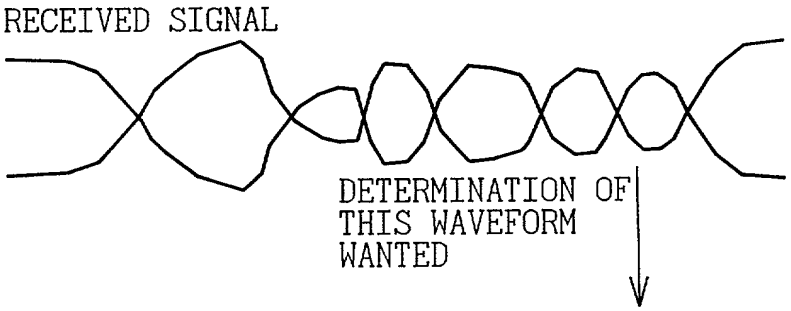


Fig.4C

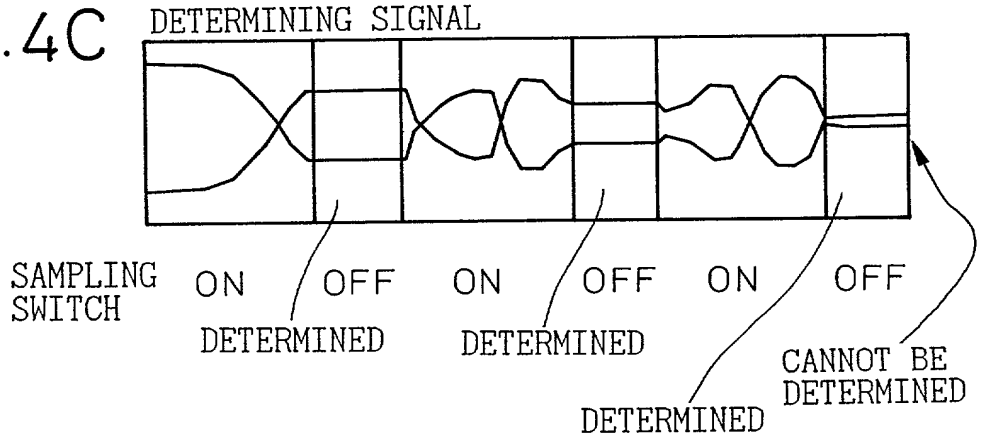


Fig.5

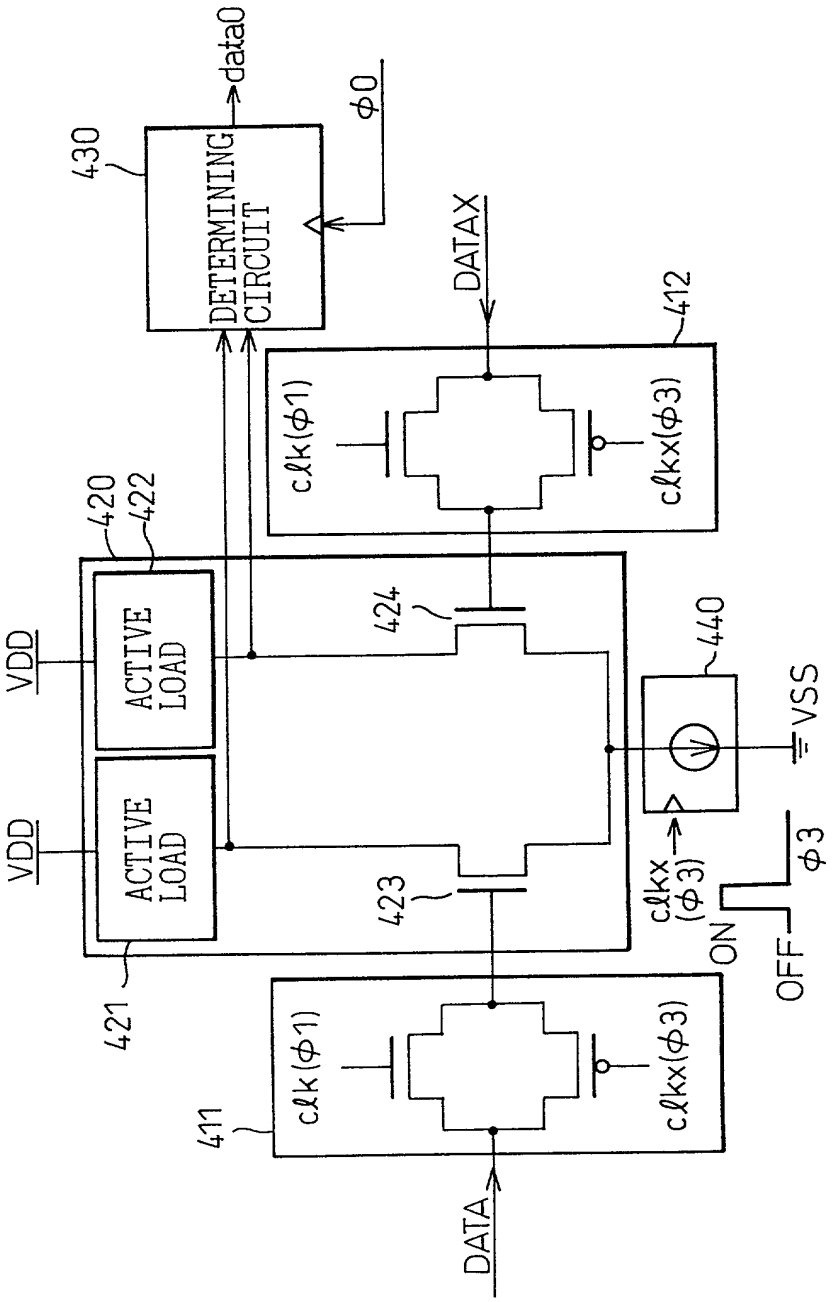

31
430
DETERMINING CIRCUIT
data0
φ0
DATAX
412
clk(φ1)
clkx(φ3)
420
422
VDD
ACTIVE LOAD
VDD
ACTIVE LOAD
424
423
421
440
VSS
clkx (φ3)
ON
OFF
φ3
411
clk(φ1)
clkx(φ3)
DATA

Fig. 6A

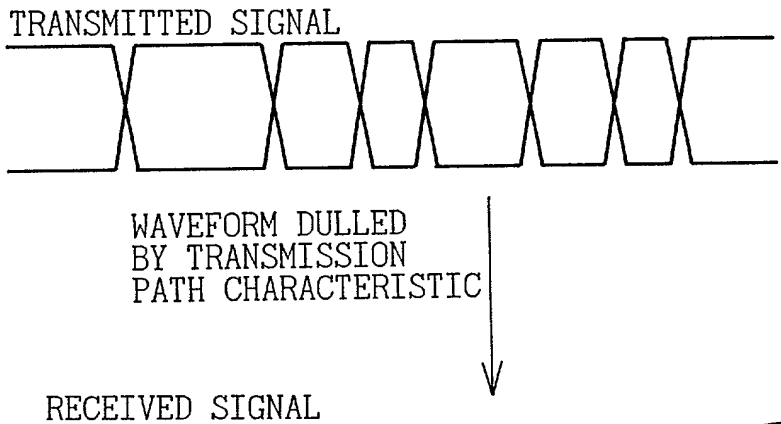


Fig. 6B

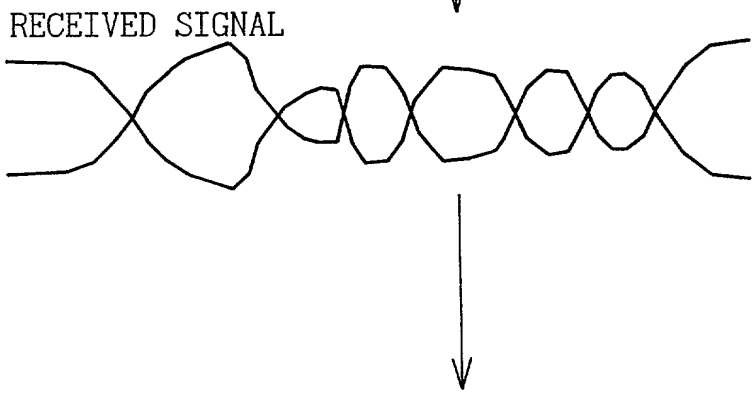


Fig. 6C

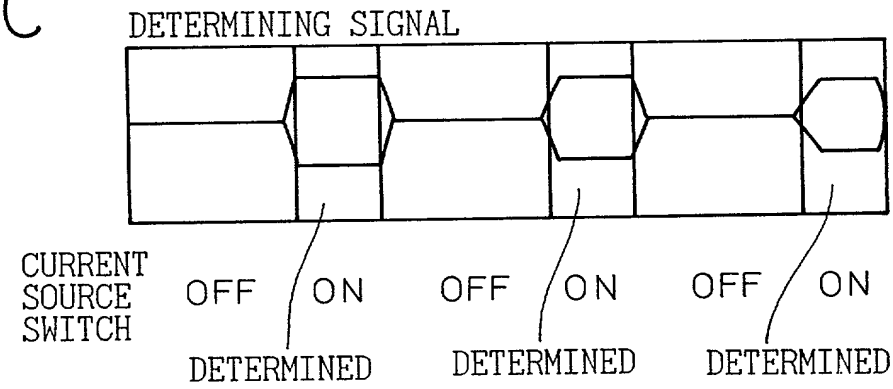


Fig.7

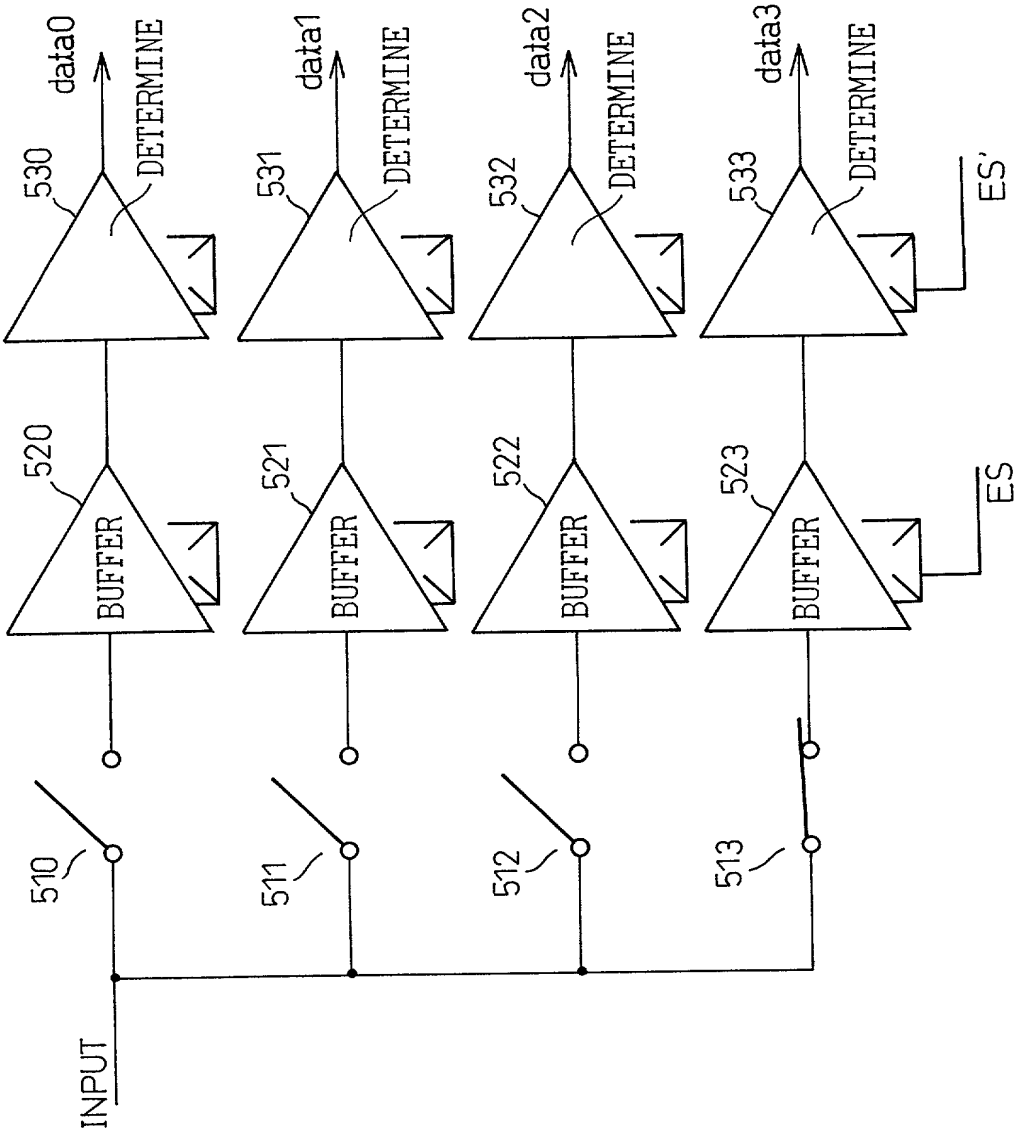

INPUT
510
511
512
513
520
521
522
523
BUFFER
530
531
532
533
DETERMINE
data0
data1
data2
data3
ES
ES'

Fig.8

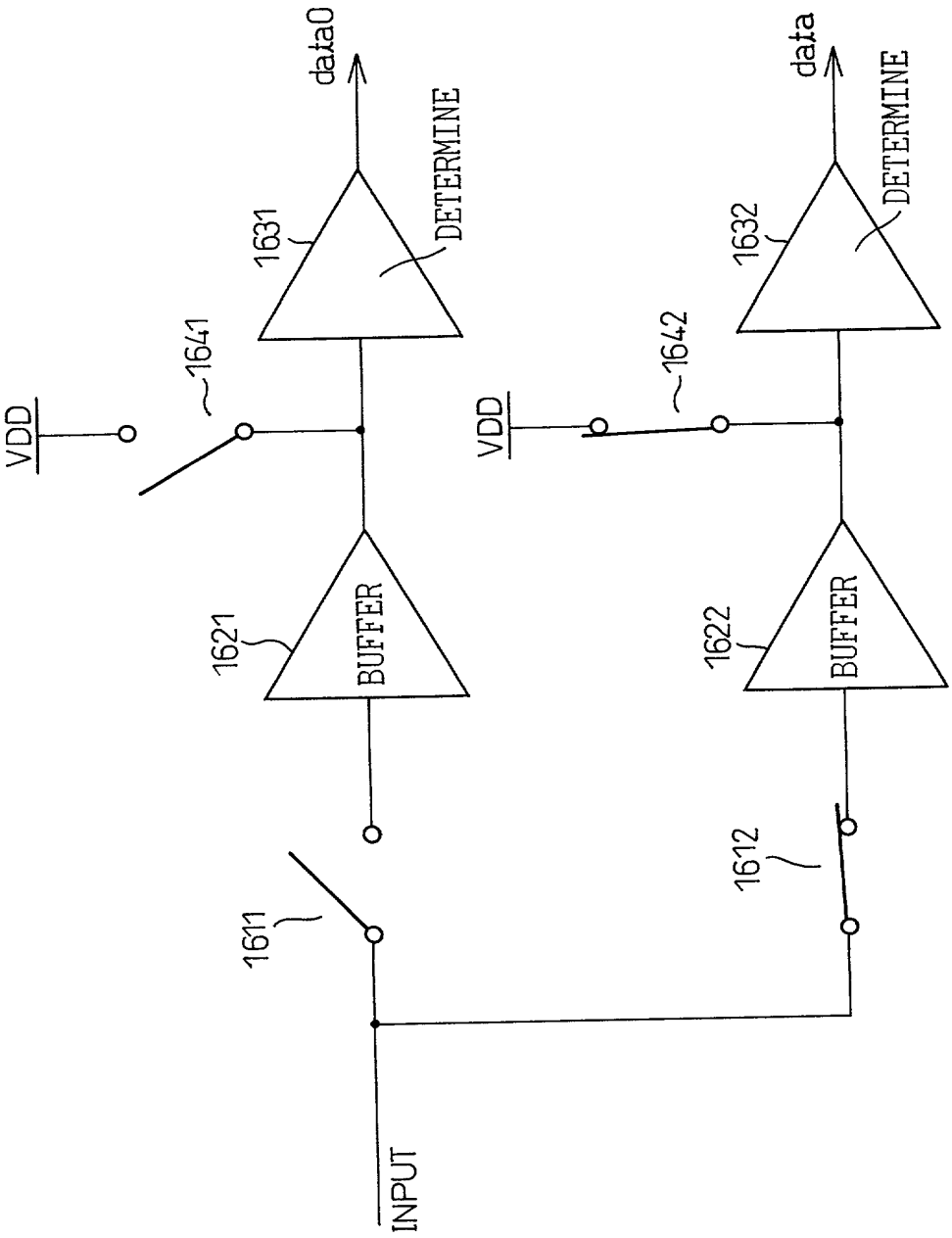

data0
DETERMINE
1631
1641
VDD
1621
BUFFER
data
DETERMINE
1632
1642
VDD
1622
BUFFER
1611
1612
INPUT

Fig.9

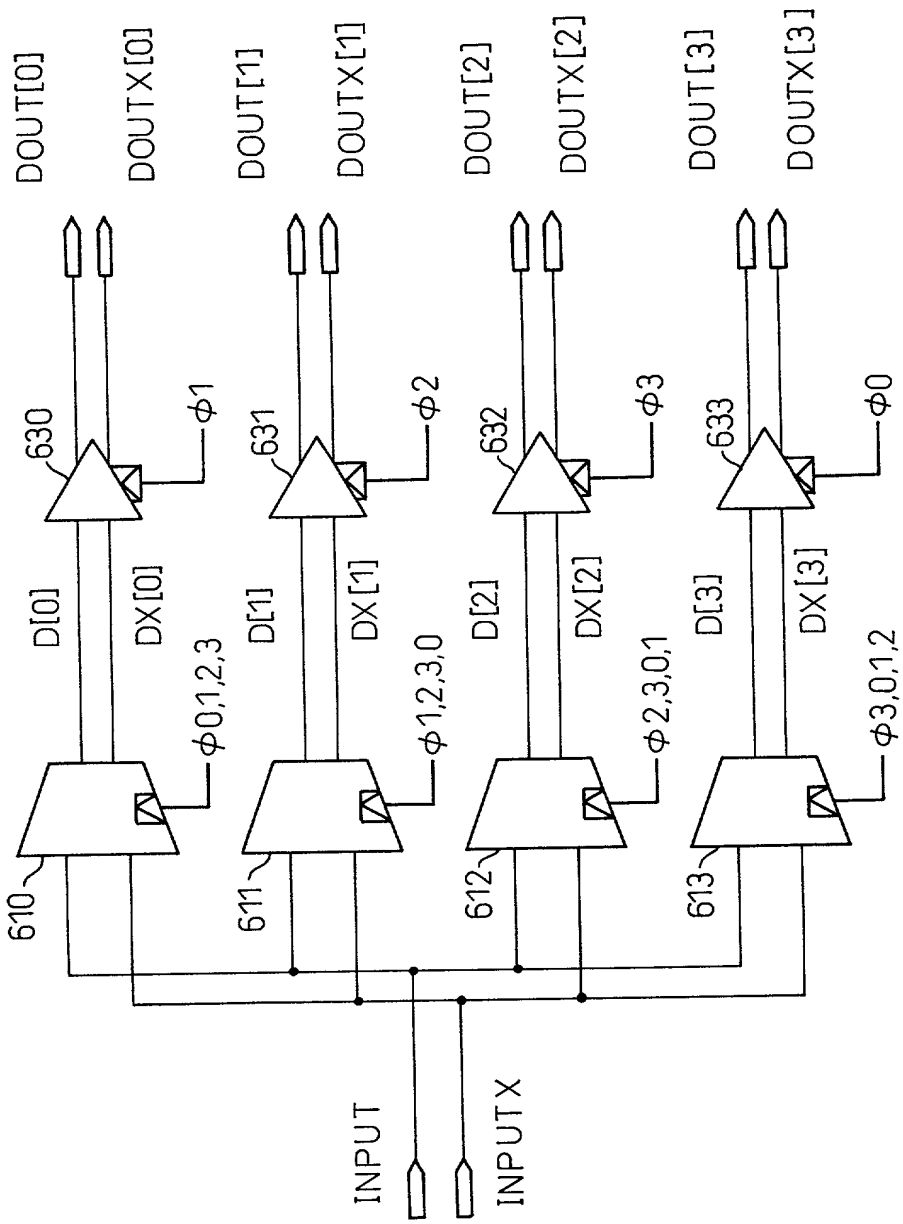

DOUT[0]
DOUTX[0]
DOUT[1]
DOUTX[1]
DOUT[2]
DOUTX[2]
DOUT[3]
DOUTX[3]
630
631
632
633
φ1
φ2
φ3
φ0
D[0]
DX[0]
D[1]
DX[1]
D[2]
DX[2]
D[3]
DX[3]
φ0,1,2,3
φ1,2,3,0
φ2,3,0,1
φ3,0,1,2
610
611
612
613
INPUT
INPUTX

Fig.10

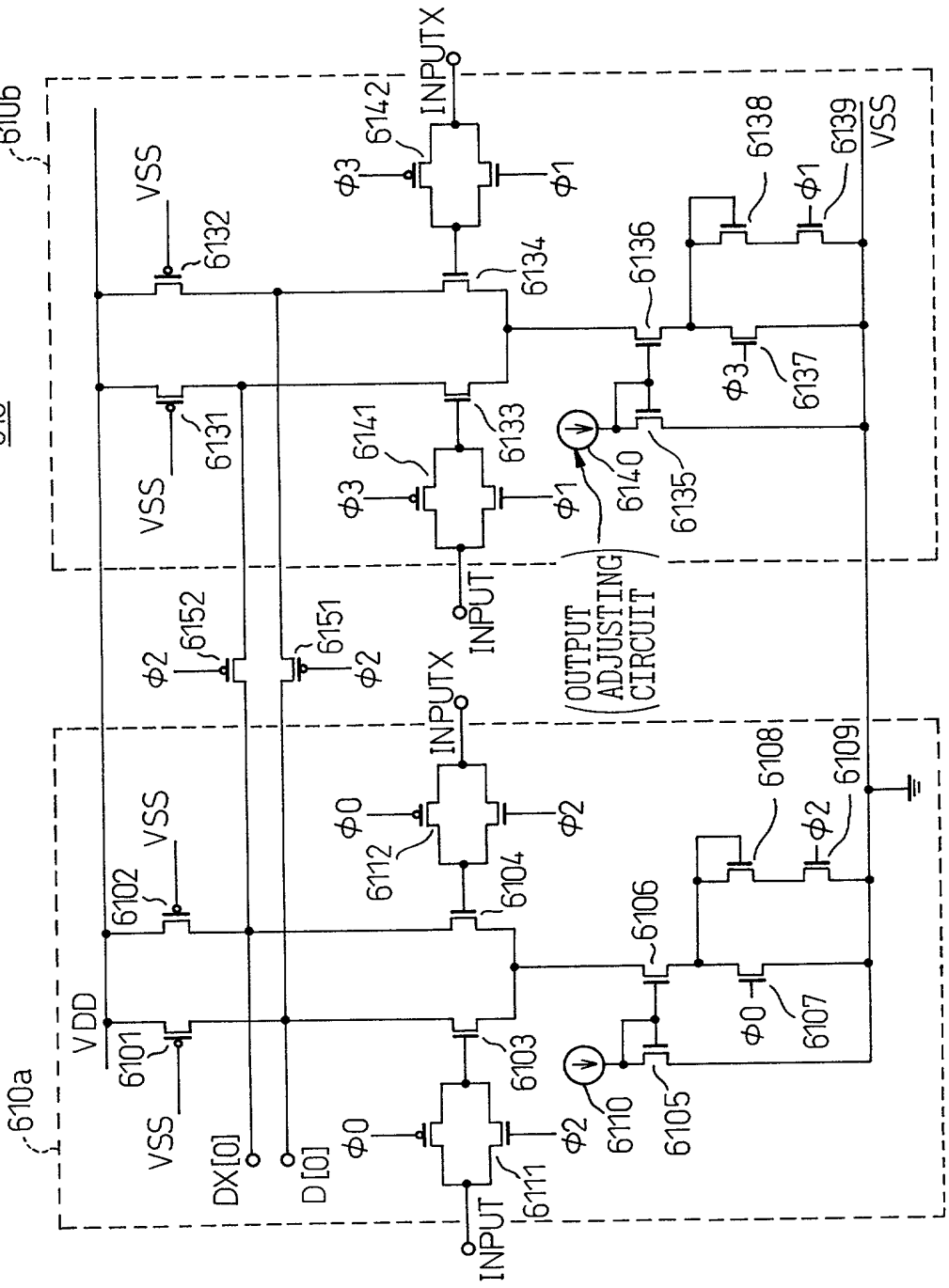

610
610a
610b
VDD
VSS
DX[0]
D[0]
INPUT
INPUTX
OUTPUT ADJUSTING CIRCUIT
6101
6102
6103
6104
6105
6106
6107
6108
6109
6110
6111
6112
6131
6132
6133
6134
6135
6136
6137
6138
6139
6140
6141
6142
6151
6152
φ0
φ1
φ2
φ3

Fig.11

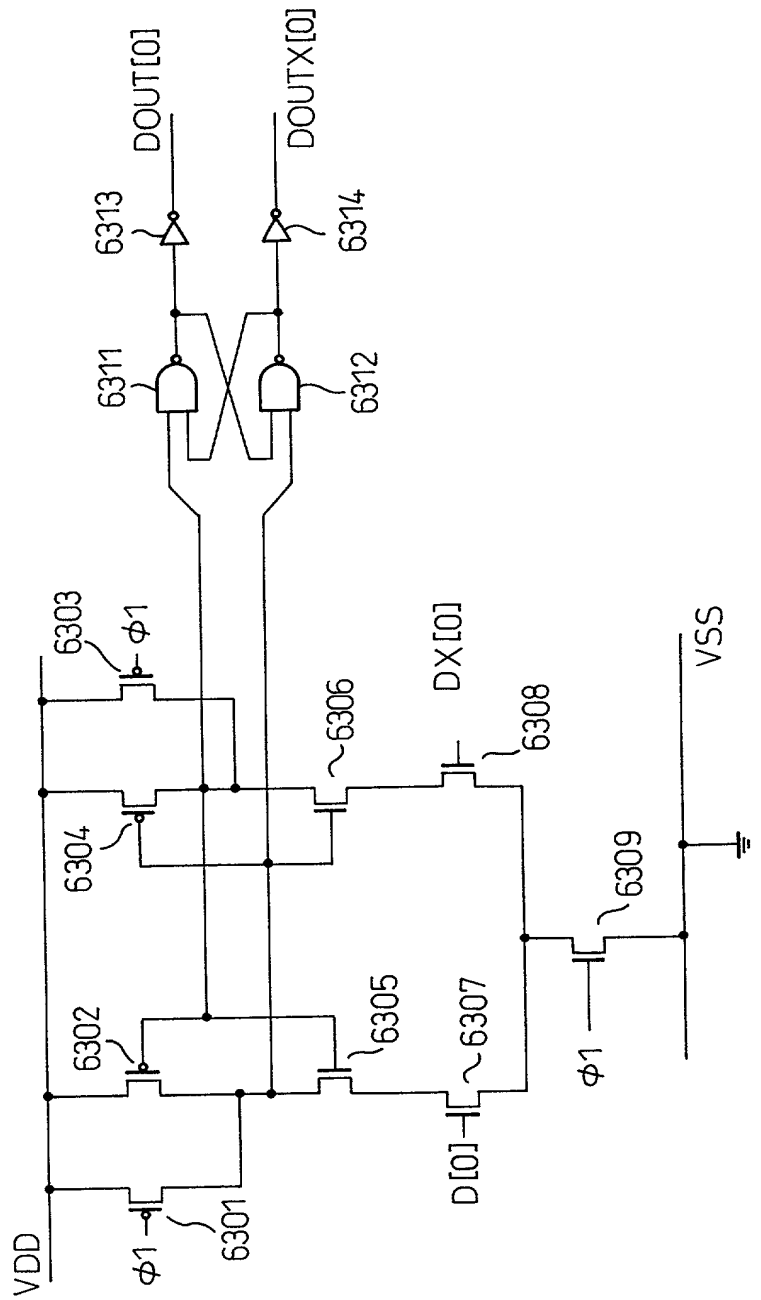
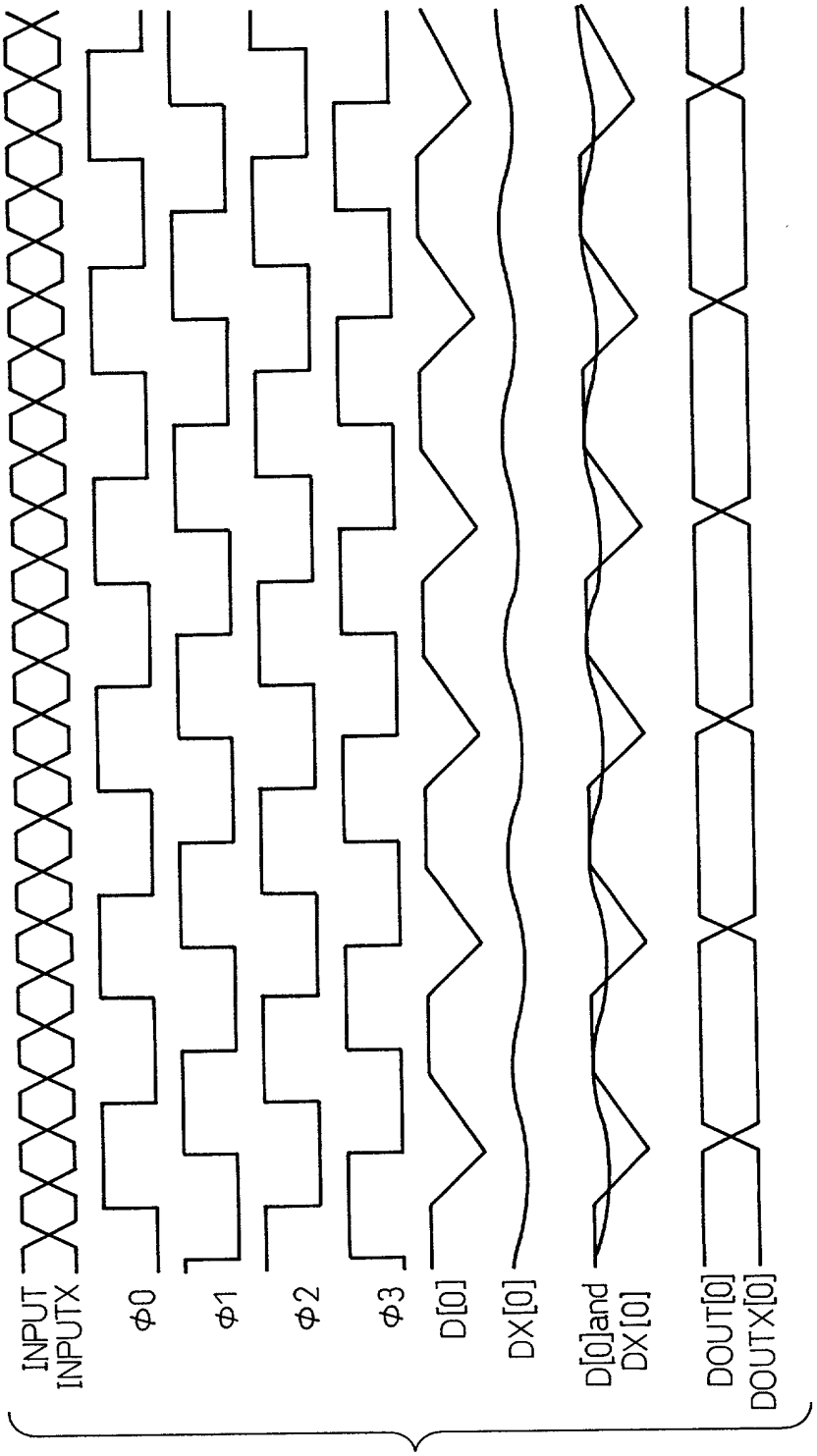

630
DOUT[0]
DOUTX[0]
6313
6314
6311
6312
6303
φ1
6306
DX[0]
6308
6304
6302
6305
6307
6309
VDD
φ1
6301
D[0]
φ1
VSS

Fig.12



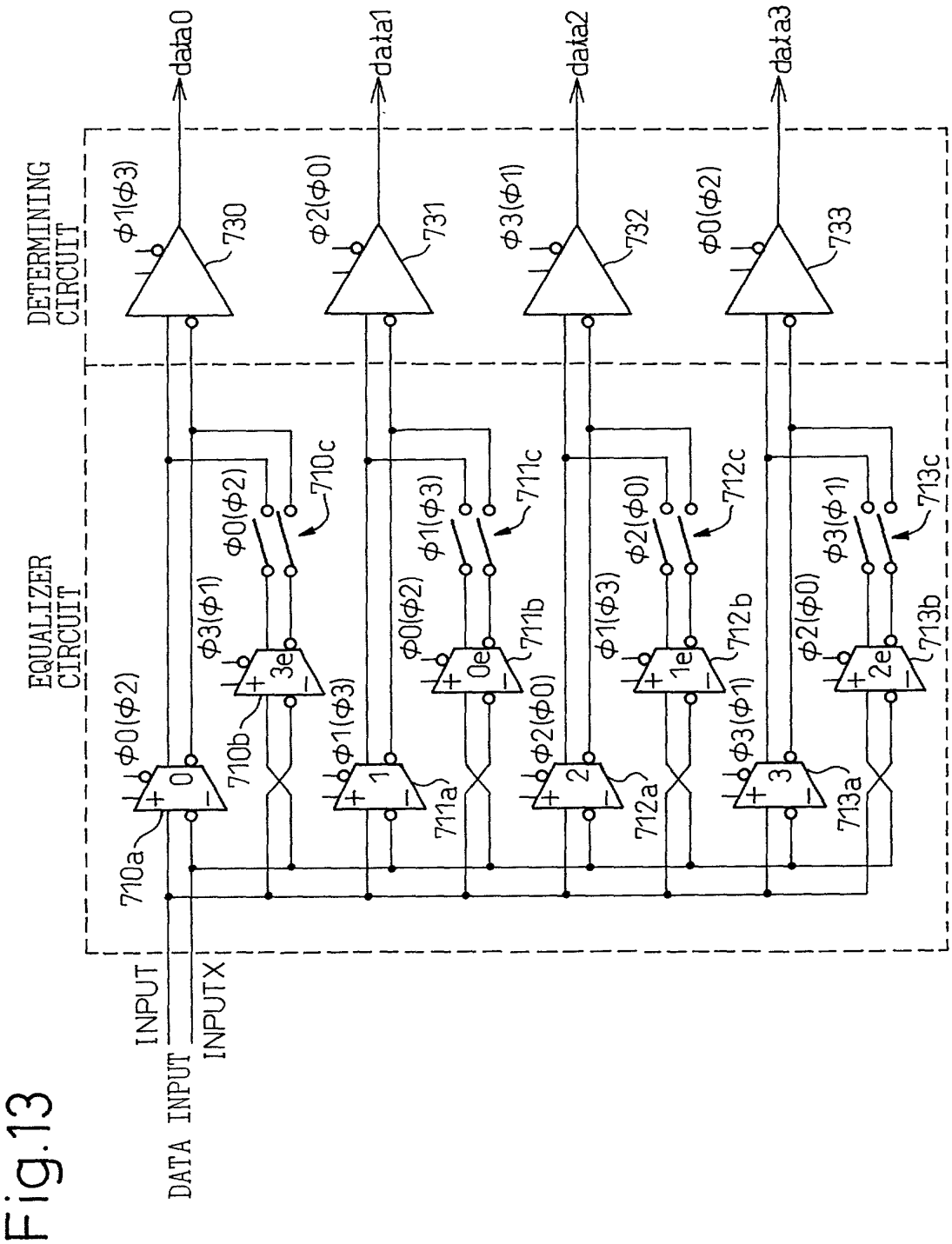

DATA INPUT
INPUT
INPUTX
EQUALIZER CIRCUIT
DETERMINING CIRCUIT
710a
710b
710c
711a
711b
711c
712a
712b
712c
713a
713b
713c
730
731
732
733
data0
data1
data2
data3
φ0(φ2)
φ1(φ3)
φ2(φ0)
φ3(φ1)
0
1
2
3
0e
1e
2e
3e

Fig.13

Fig.14

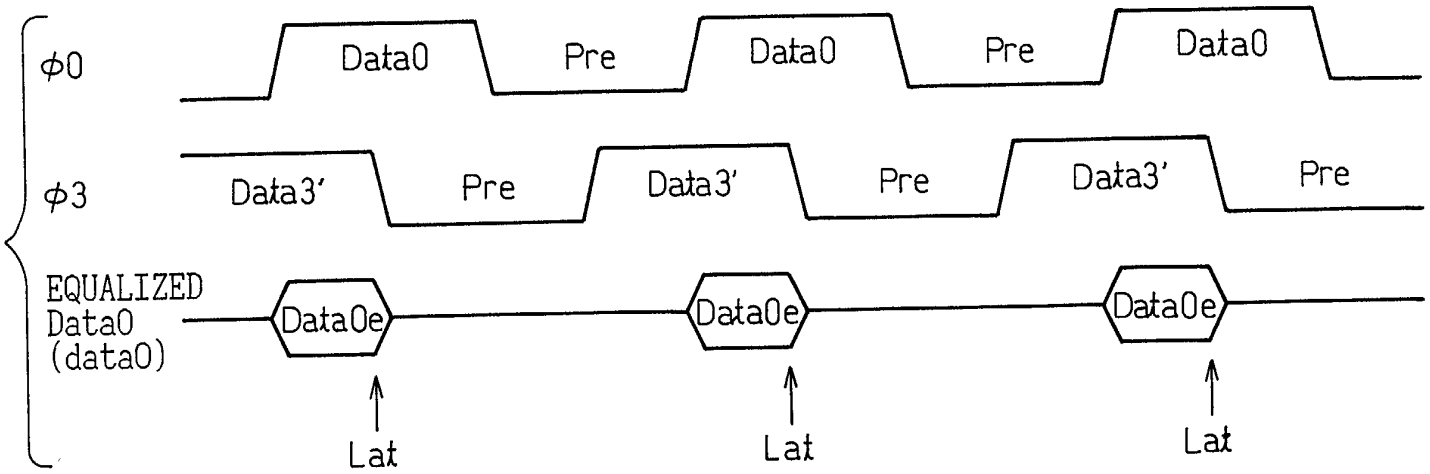

φ0
Data0
Pre
Data0
Pre
Data0
φ3
Data3'
Pre
Data3'
Pre
Data3'
Pre
EQUALIZED
Data0
(data0)
Data0e
Data0e
Data0e
Lat
Lat
Lat

Fig.15

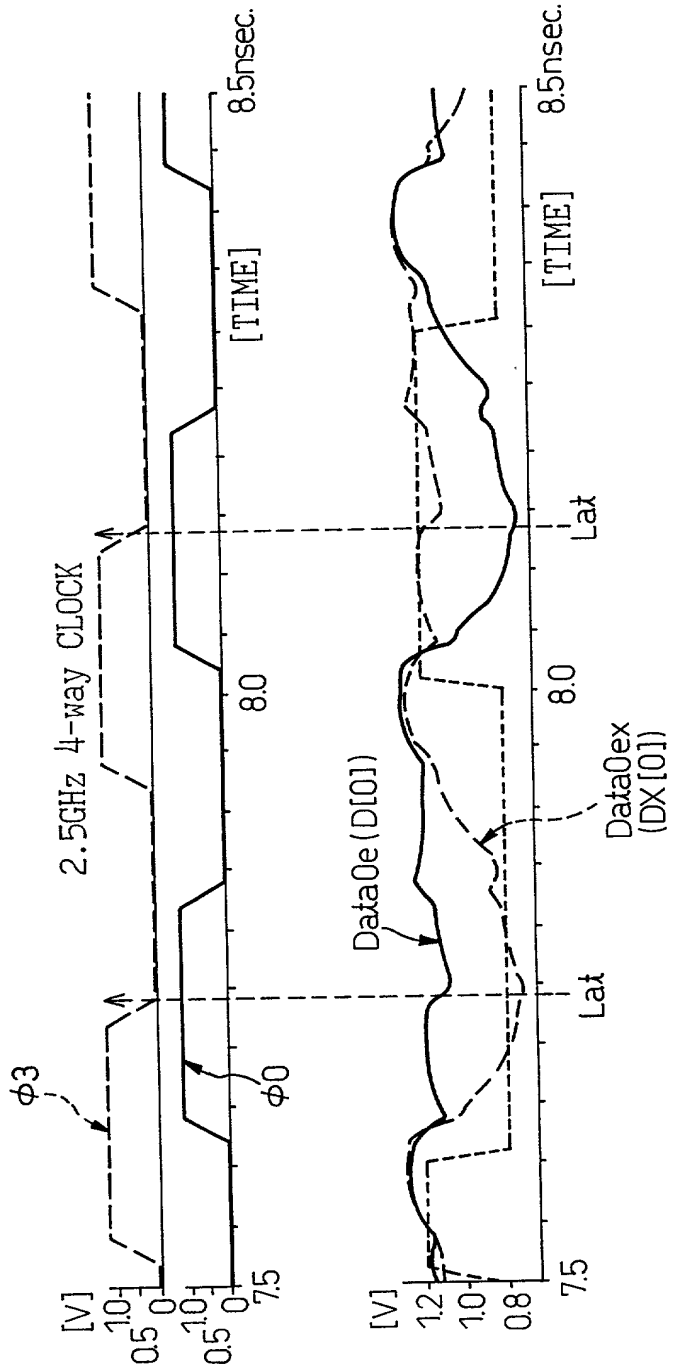

2.5GHz 4-way CLOCK
φ3
φ0
[V]
1.0
0.5
0
7.5
8.0
8.5nsec.
[TIME]
Lat
Data0e (DI01)
Data0ex (DX[01])
1.2
0.8

Fig.16

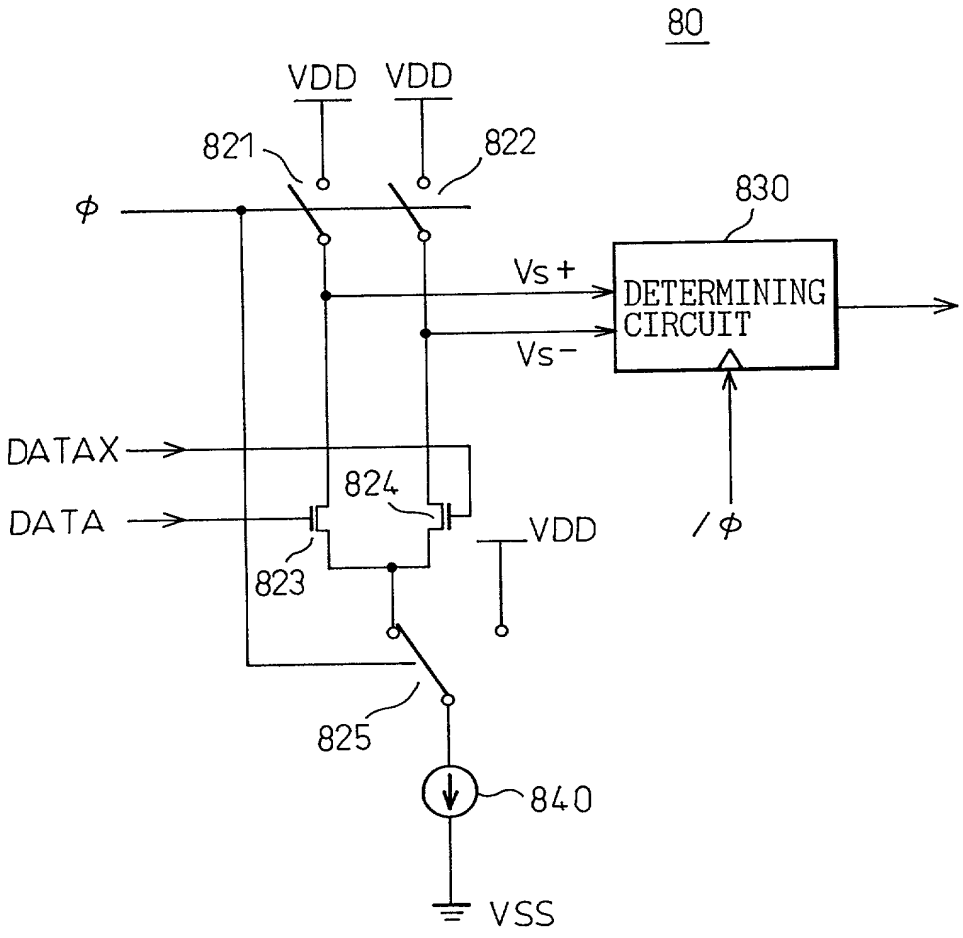

80
VDD
VDD
821
822
φ
830
Vs+
DETERMINING CIRCUIT
Vs−
DATAX
DATA
824
VDD
/φ
823
825
840
VSS

Fig.17

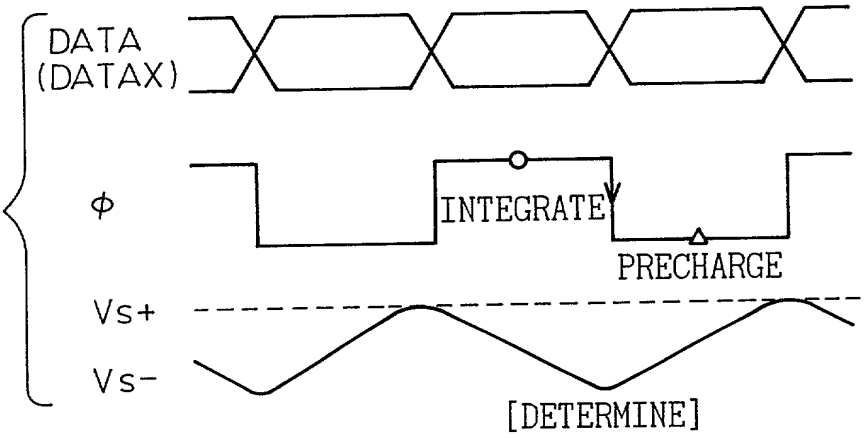


Fig.18

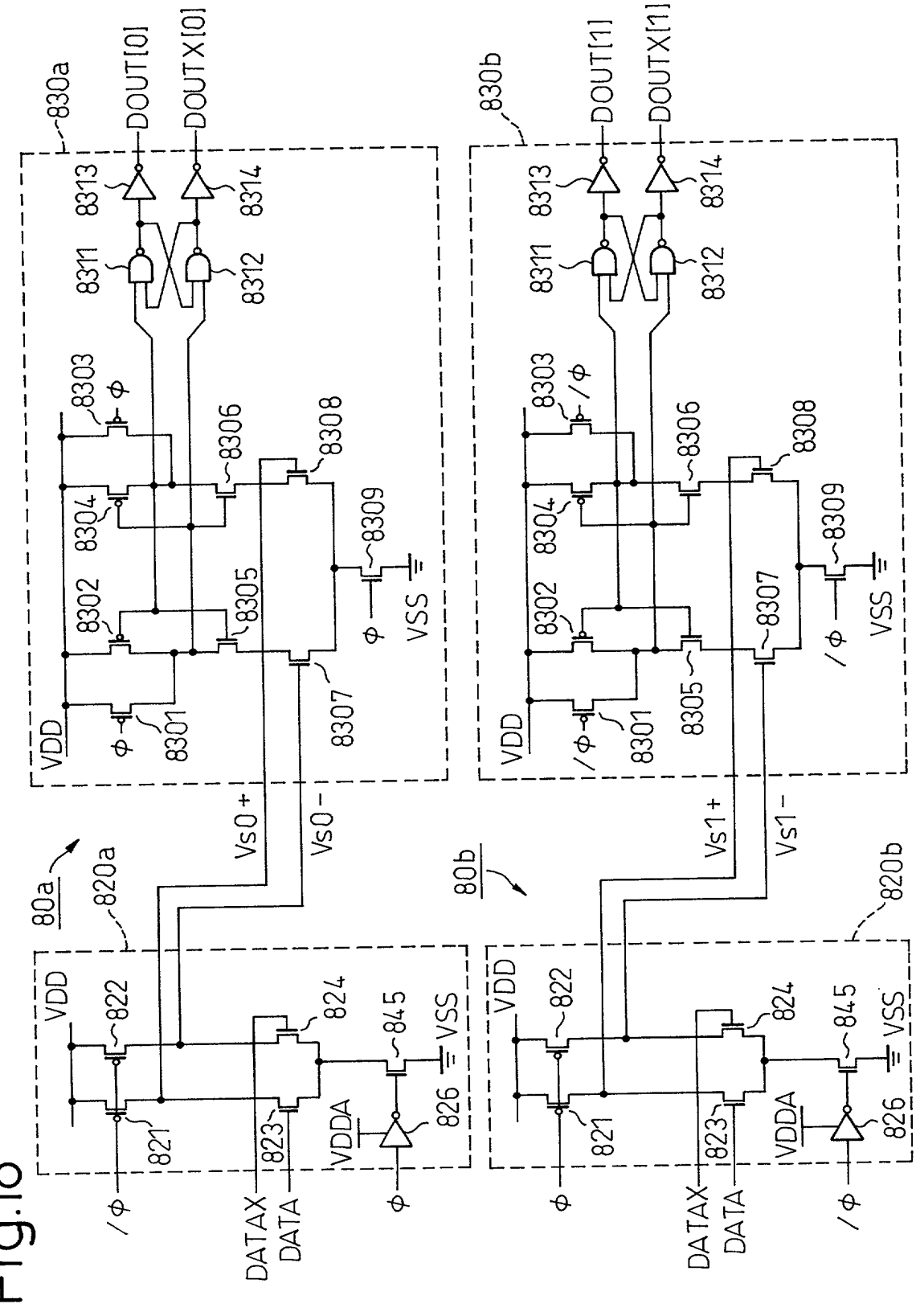

80a
820a
VDD
822
821
823
824
826
845
VSS
VDDA
/φ
φ
DATAX
DATA
Vs0+
Vs0−
830a
DOUT[0]
DOUTX[0]
8301
8302
8303
8304
8305
8306
8307
8308
8309
8311
8312
8313
8314
80b
820b
Vs1+
Vs1−
830b
DOUT[1]
DOUTX[1]

Fig.19

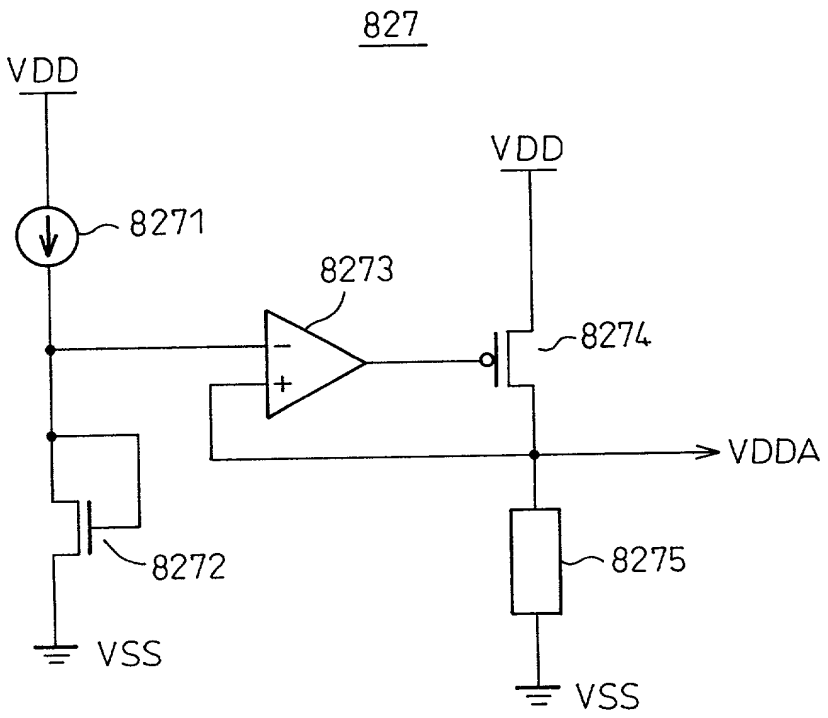


Fig.20

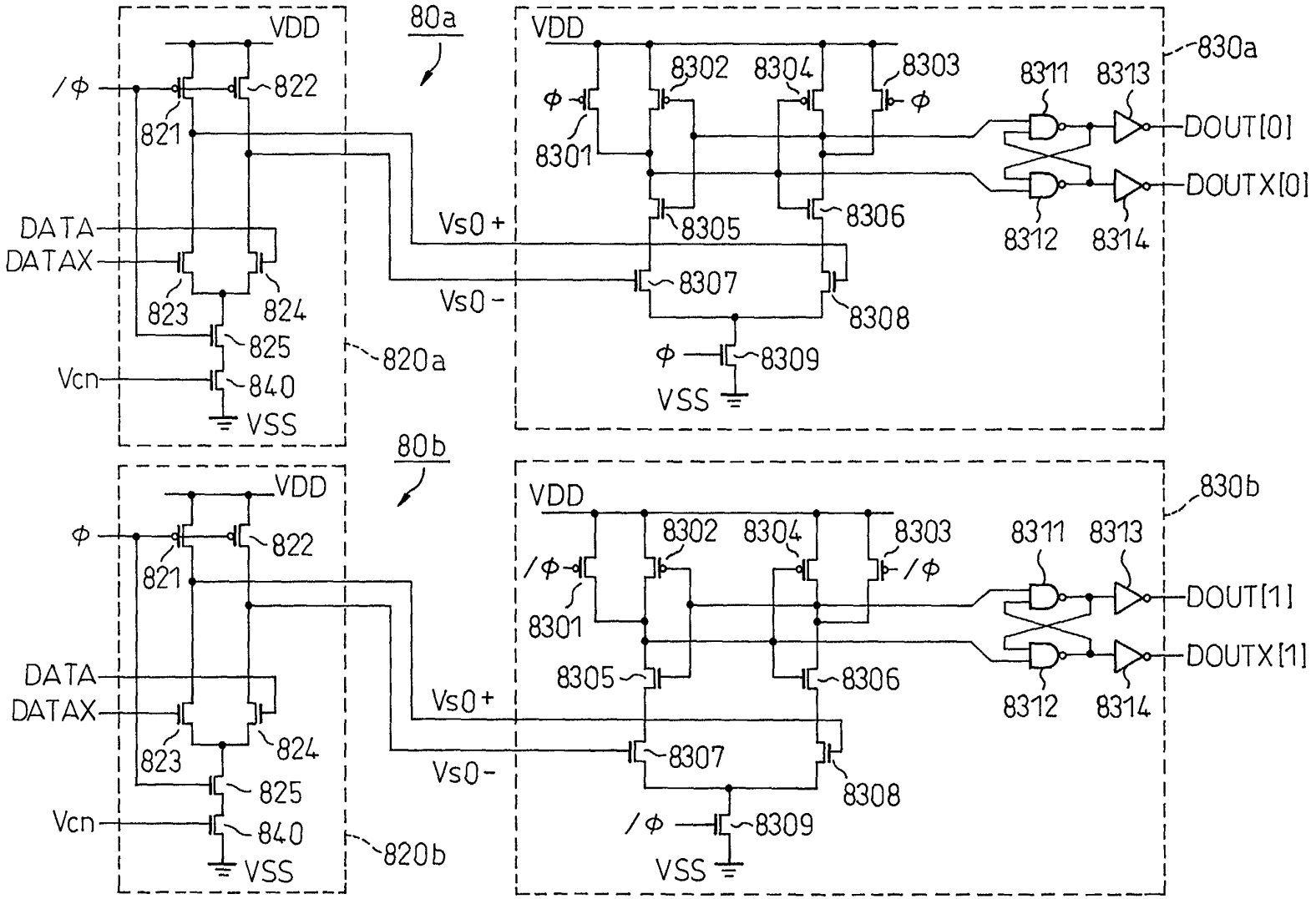

80a
VDD
/φ
822
821
DATA
DATAX
823
824
825
Vcn
840
VSS
820a
Vs0+
Vs0-
8302
8304
8303
8301
8305
8306
8307
8308
8309
8311
8313
8312
8314
830a
DOUT[0]
DOUTX[0]
80b
φ
820b
830b
DOUT[1]
DOUTX[1]

Fig.21

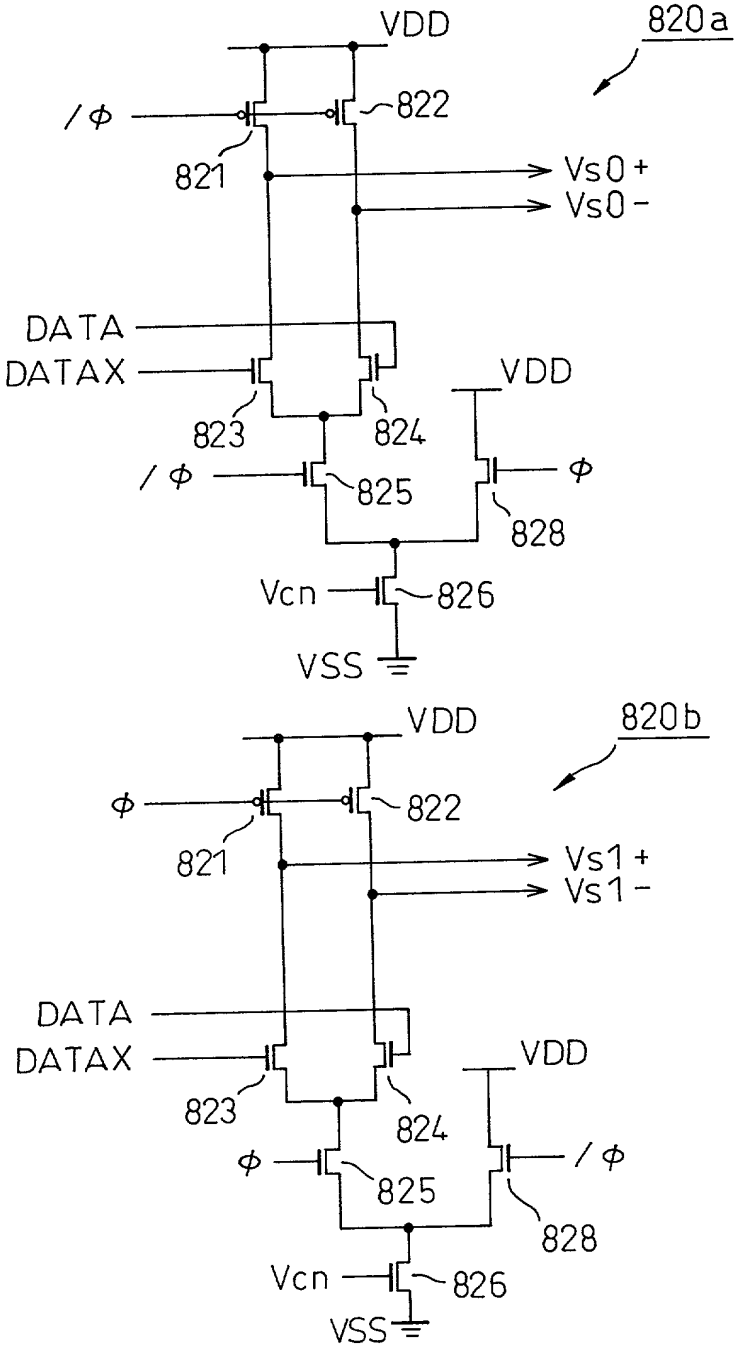

820a
VDD
/φ
822
821
Vs0+
Vs0-
DATA
DATAX
823
824
VDD
/φ
825
φ
828
Vcn
826
VSS
820b
VDD
φ
822
821
Vs1+
Vs1-
DATA
DATAX
823
824
VDD
φ
825
/φ
828
Vcn
826
VSS

Fig. 22

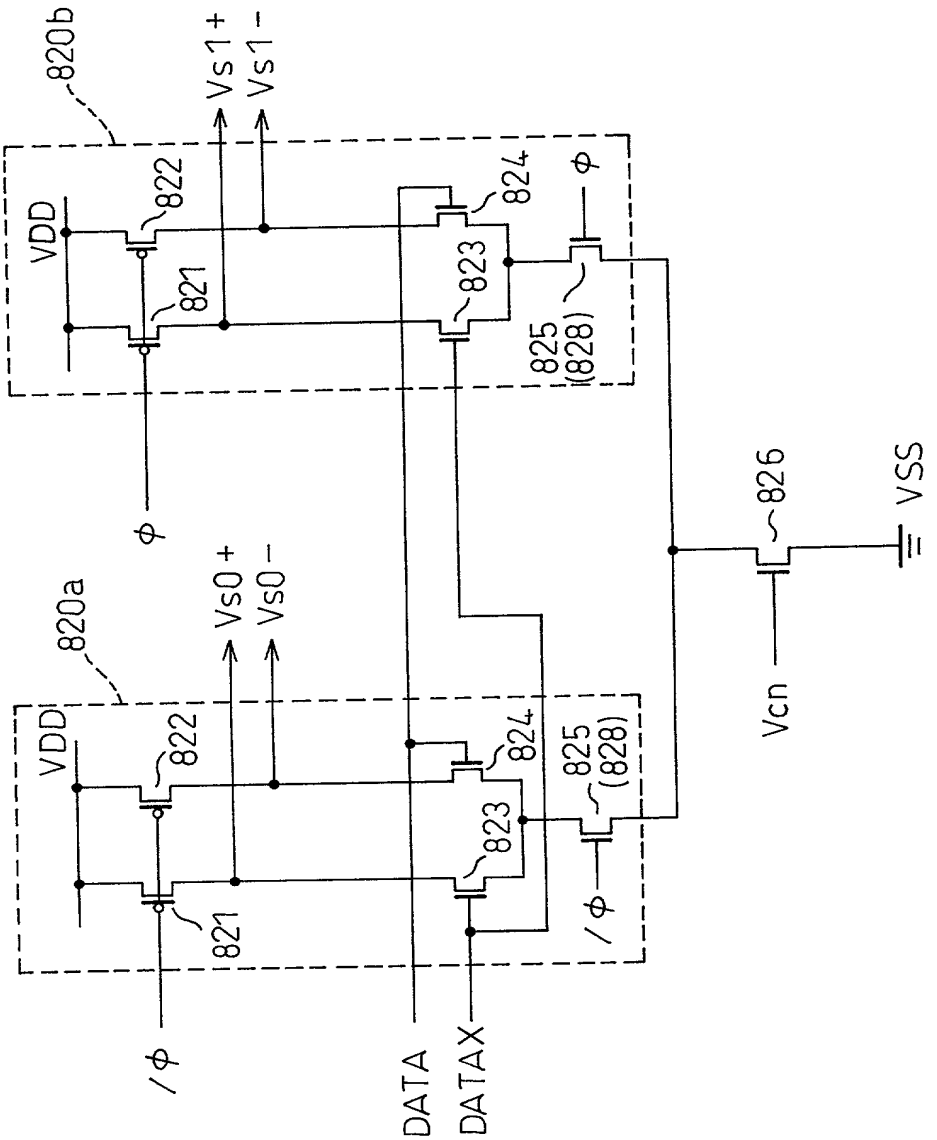

820b
Vs1+
Vs1−
VDD
822
821
823
824
825
(828)
φ
826
VSS
Vcn
820a
Vs0+
Vs0−
/φ
DATA
DATAX

Fig.23

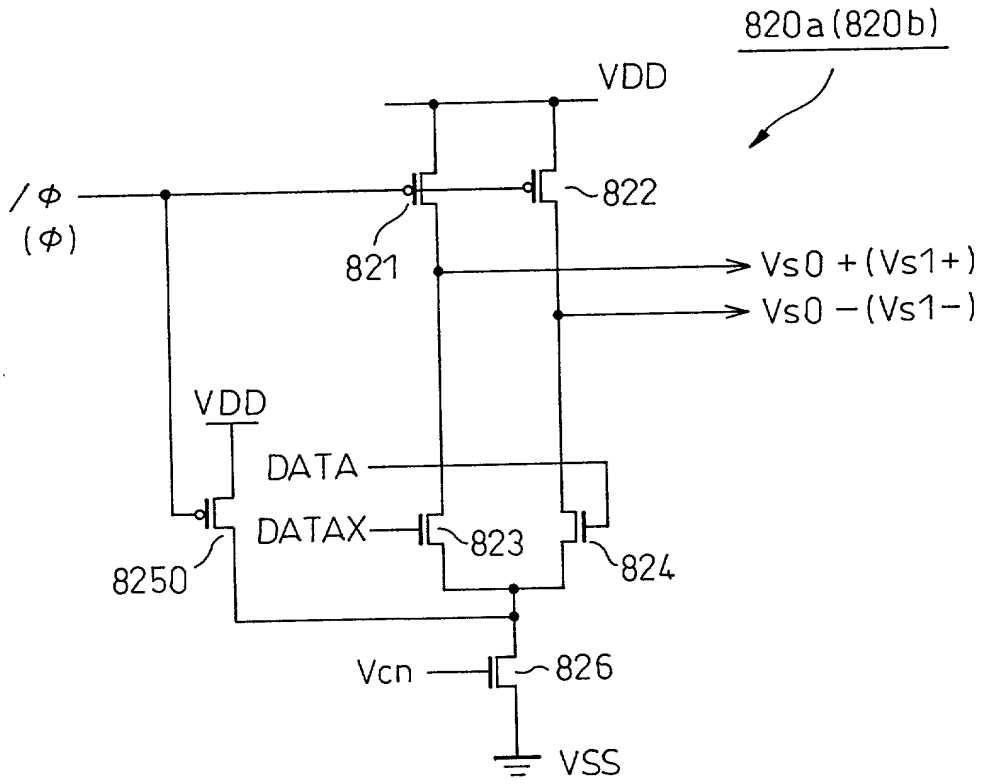

820a(820b)
VDD
/Φ
(Φ)
822
821
Vs0 +(Vs1+)
Vs0 −(Vs1−)
VDD
DATA
DATAX
823
824
8250
Vcn
826
VSS

Fig. 24

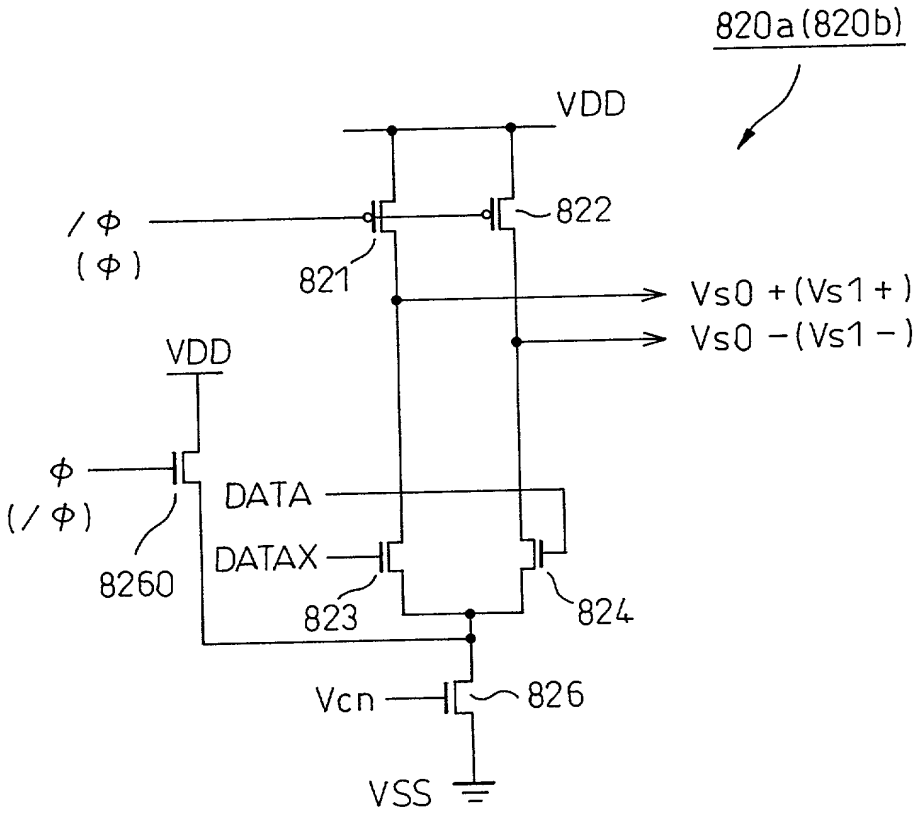

820a(820b)
VDD
/Φ
(Φ)
821
822
Vs0+(Vs1+)
Vs0−(Vs1−)
VDD
Φ
(/Φ)
8260
DATA
DATAX
823
824
Vcn
826
VSS

Fig. 25

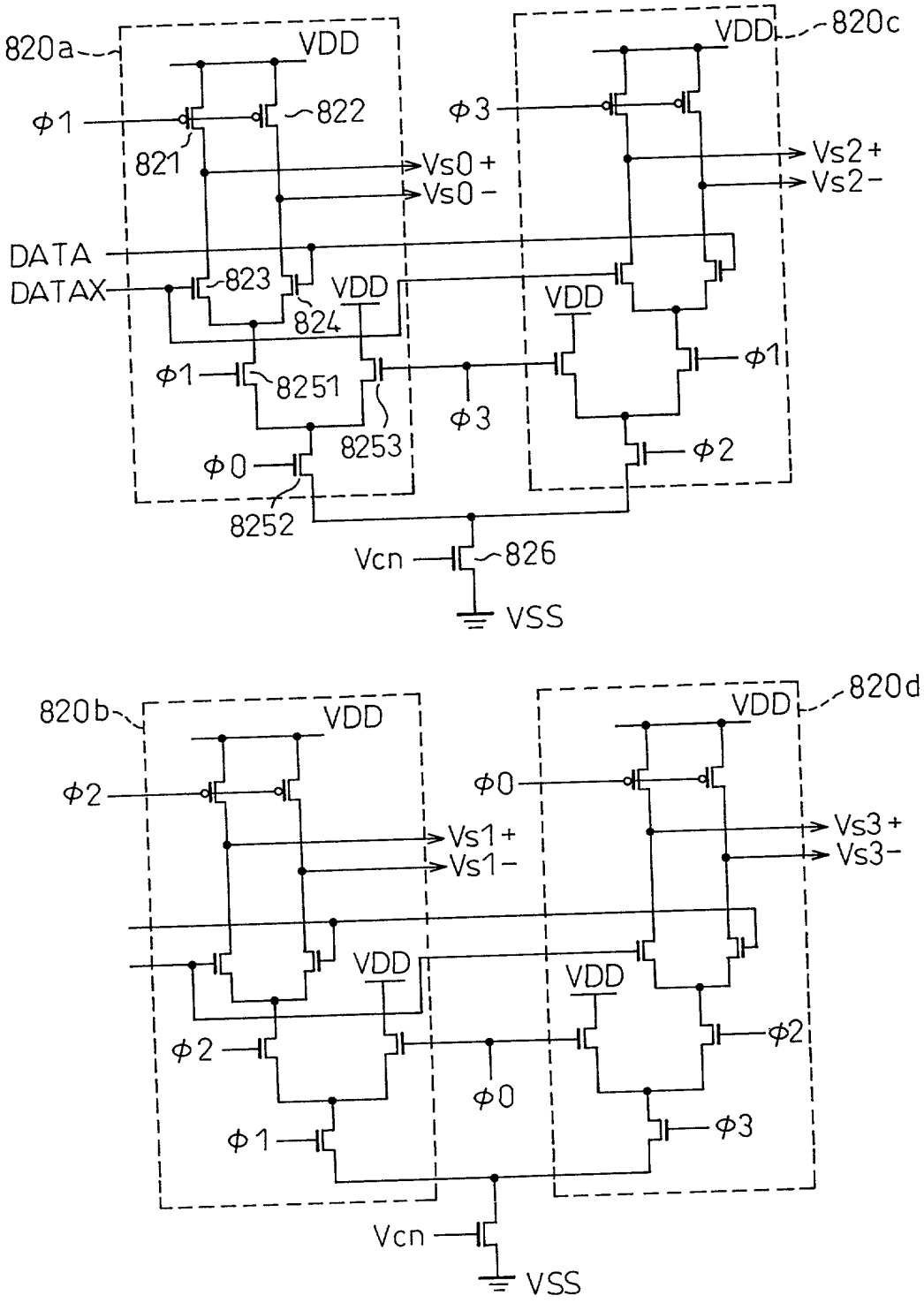

820a
VDD
φ1
822
821
Vs0+
Vs0−
DATA
DATAX
823
824
VDD
φ1
8251
8253
φ0
8252
φ3
820c
VDD
φ3
Vs2+
Vs2−
VDD
φ1
φ2
Vcn
826
VSS
820b
VDD
φ2
Vs1+
Vs1−
VDD
φ2
φ1
φ0
820d
VDD
φ0
Vs3+
Vs3−
VDD
φ2
φ3
Vcn
VSS

Fig.26

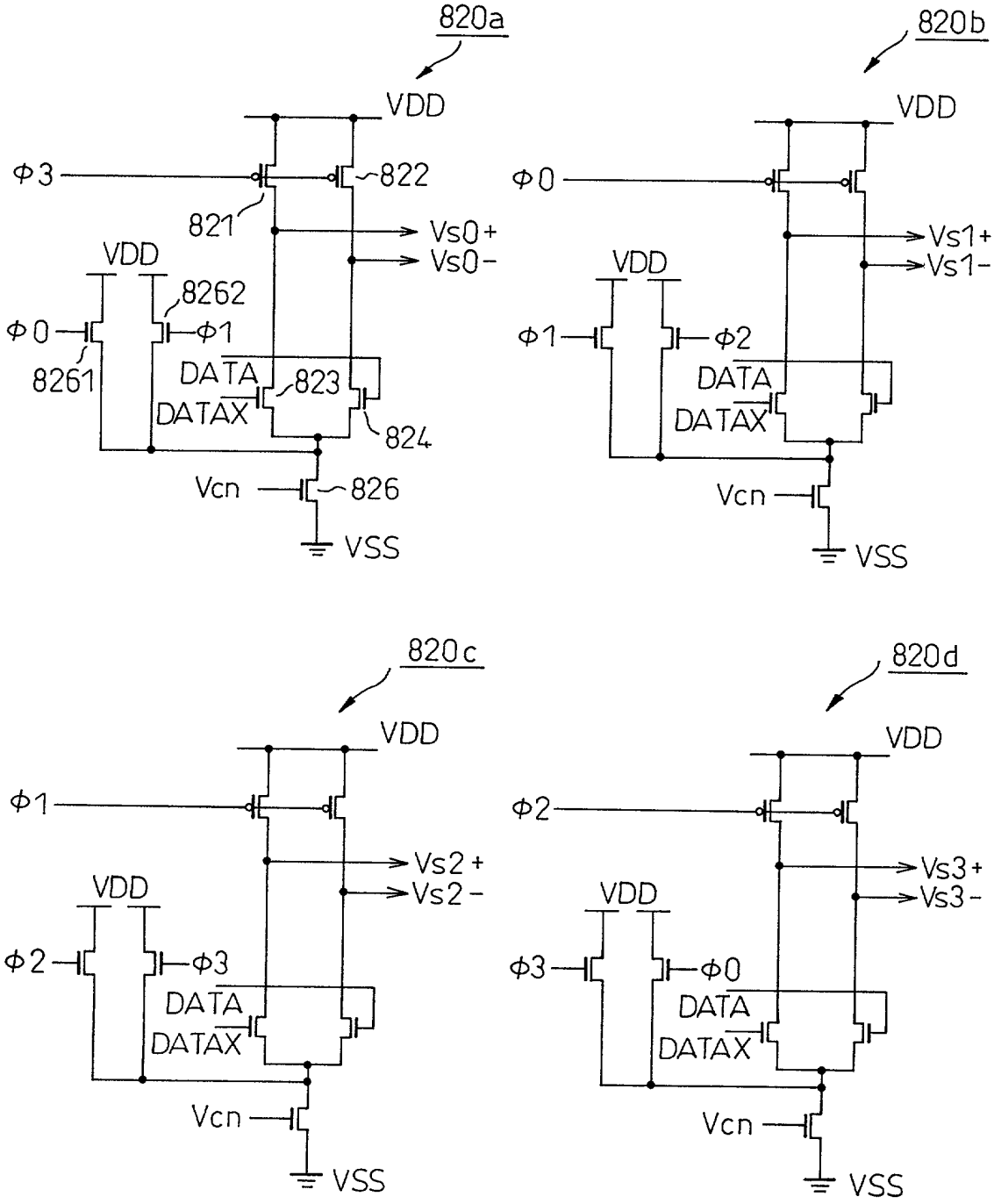

820a
VDD
Φ3
822
821
Vs0+
Vs0-
VDD
8262
Φ0
Φ1
8261
DATA
823
DATAX
824
Vcn
826
VSS
820b
VDD
Φ0
Vs1+
Vs1-
VDD
Φ1
Φ2
DATA
DATAX
Vcn
VSS
820c
VDD
Φ1
Vs2+
Vs2-
VDD
Φ2
Φ3
DATA
DATAX
Vcn
VSS
820d
VDD
Φ2
Vs3+
Vs3-
VDD
Φ3
Φ0
DATA
DATAX
Vcn
VSS

Fig.27

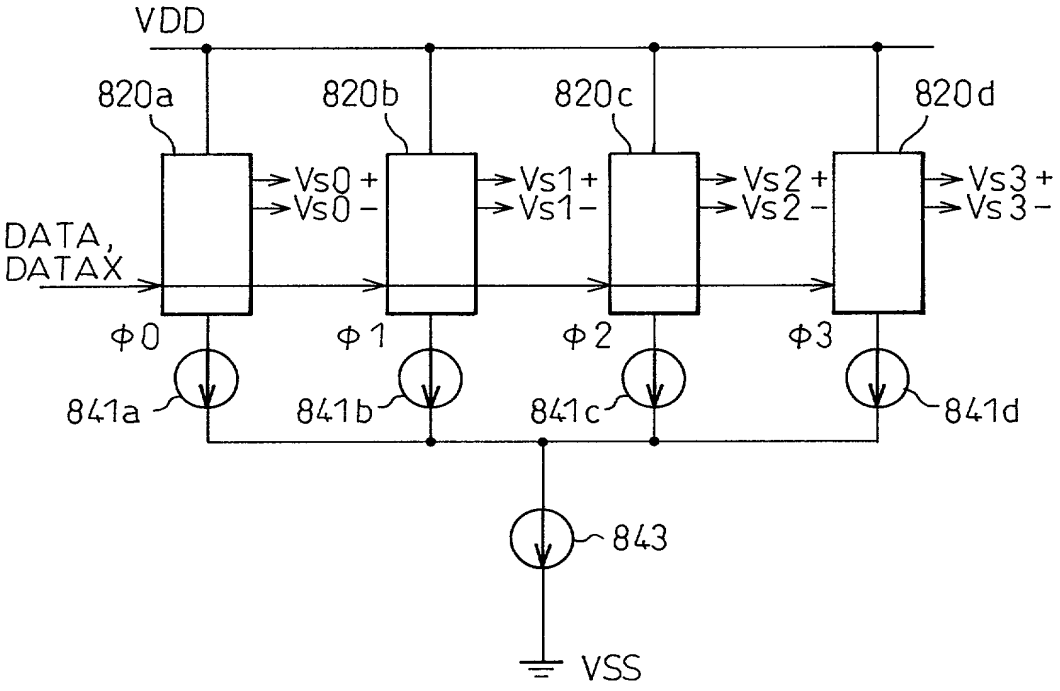

VDD
820a
820b
820c
820d
Vs0+
Vs0−
Vs1+
Vs1−
Vs2+
Vs2−
Vs3+
Vs3−
DATA,
DATAX
Φ0
Φ1
Φ2
Φ3
841a
841b
841c
841d
843
VSS

Fig.28

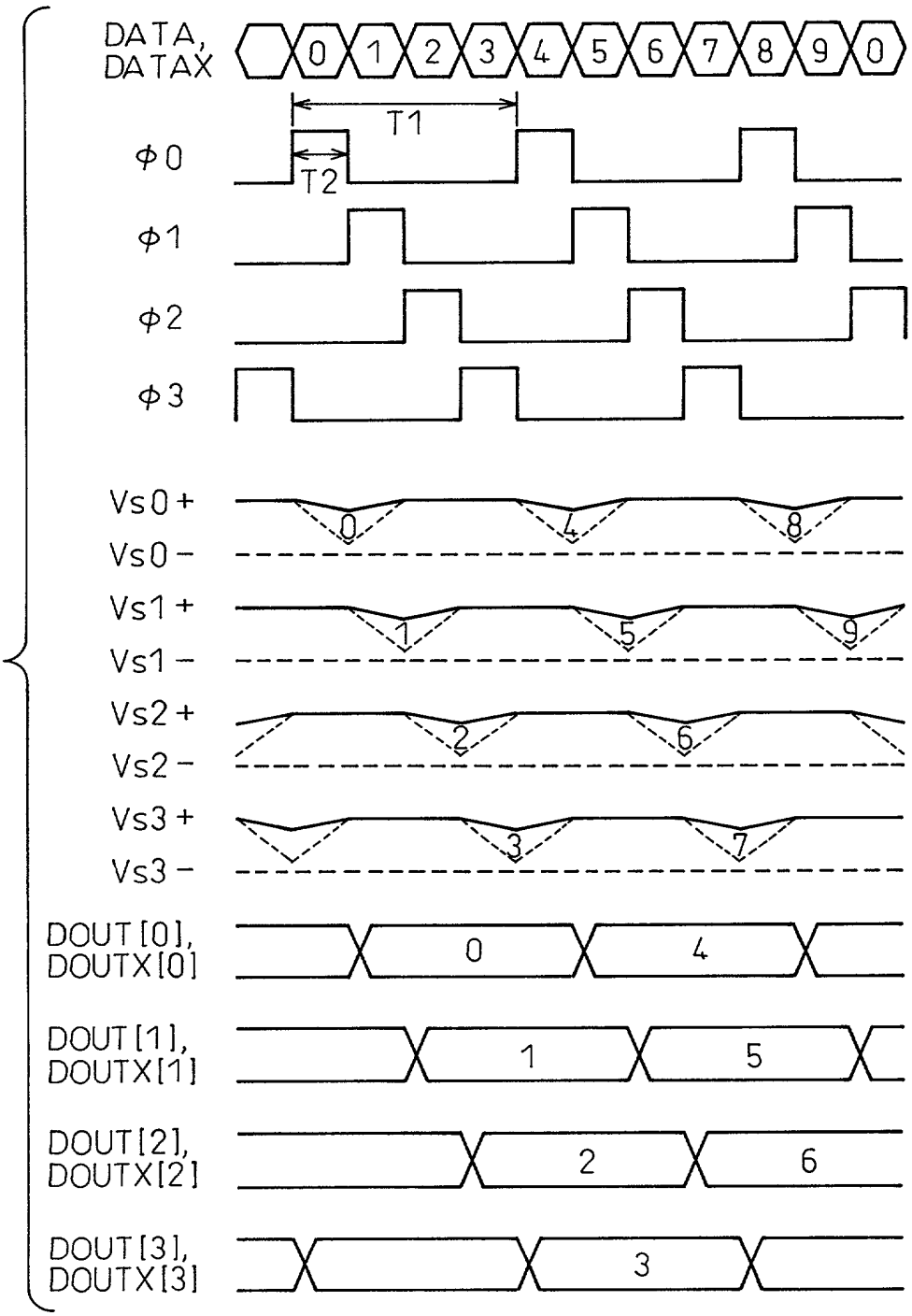

DATA,
DATAX
0 1 2 3 4 5 6 7 8 9 0
T1
T2
φ0
φ1
φ2
φ3
Vs0+
Vs0−
Vs1+
Vs1−
Vs2+
Vs2−
Vs3+
Vs3−
0 4 8
1 5 9
2 6
3 7
DOUT[0],
DOUTX[0]
DOUT[1],
DOUTX[1]
DOUT[2],
DOUTX[2]
DOUT[3],
DOUTX[3]
0 4
1 5
2 6
3

Fig.29

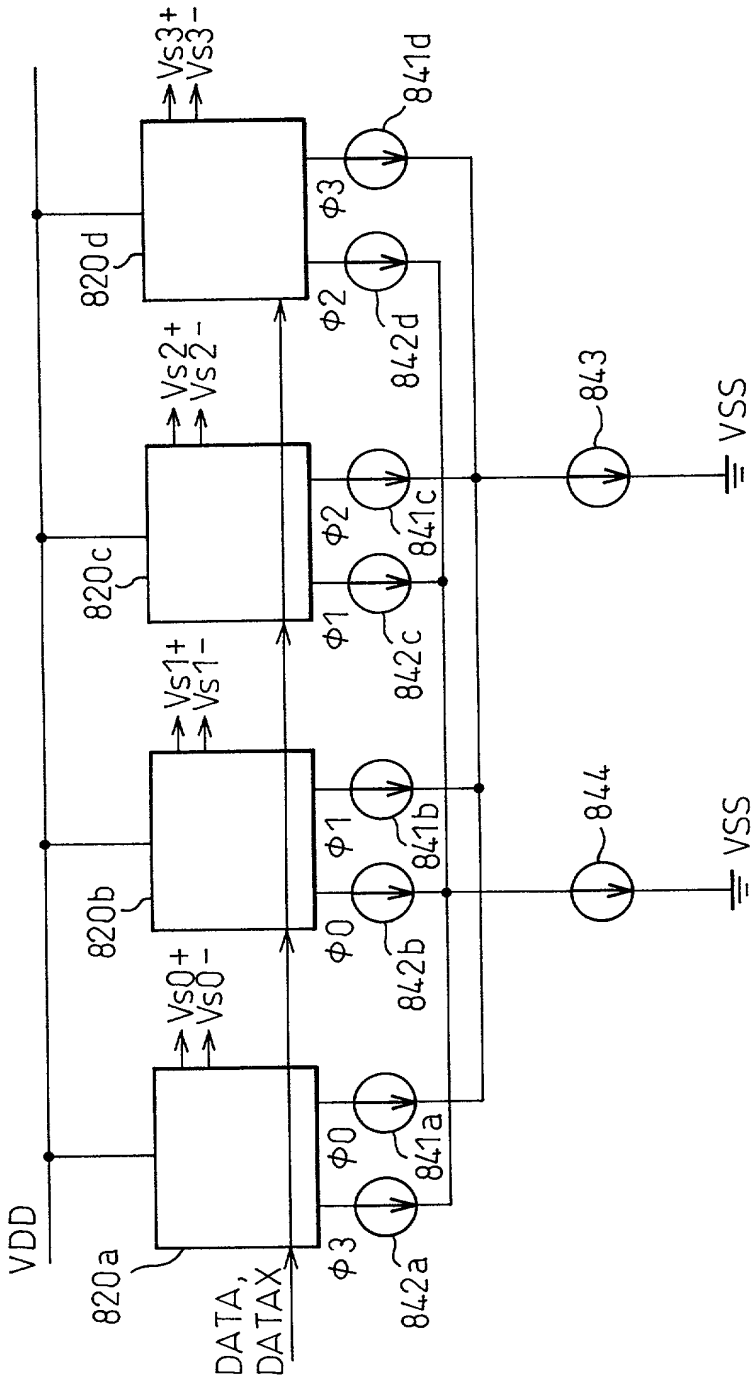

VDD
820a
820b
820c
820d
DATA,
DATAX
Vs0+
Vs0-
Vs1+
Vs1-
Vs2+
Vs2-
Vs3+
Vs3-
φ0
φ1
φ2
φ3
841a
841b
841c
841d
842a
842b
842c
842d
843
844
VSS
VSS

Fig.30

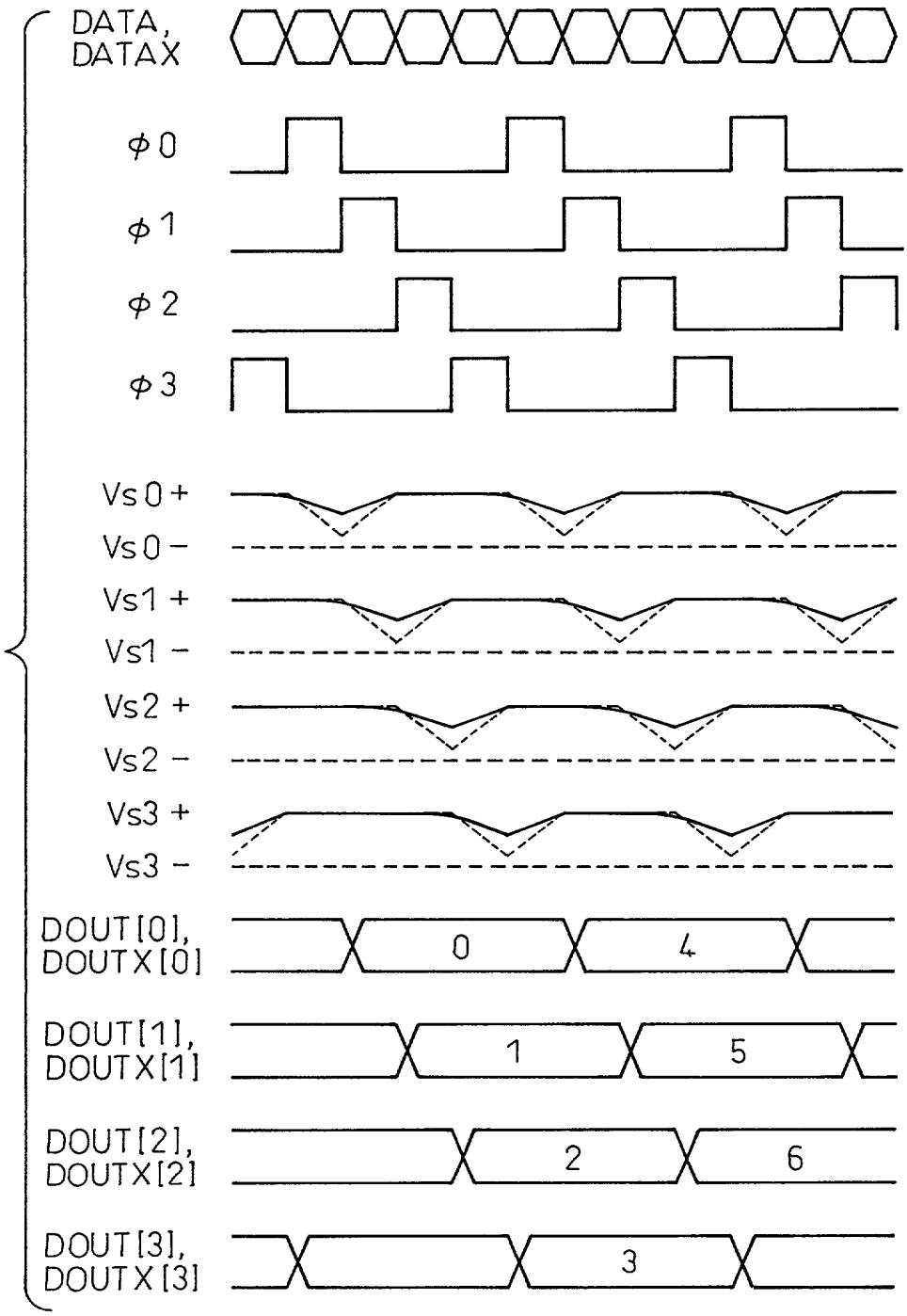

DATA,
DATAX
φ0
φ1
φ2
φ3
Vs0+
Vs0−
Vs1+
Vs1−
Vs2+
Vs2−
Vs3+
Vs3−
DOUT[0],
DOUTX[0]
0
4
DOUT[1],
DOUTX[1]
1
5
DOUT[2],
DOUTX[2]
2
6
DOUT[3],
DOUTX[3]
3

Fig.31

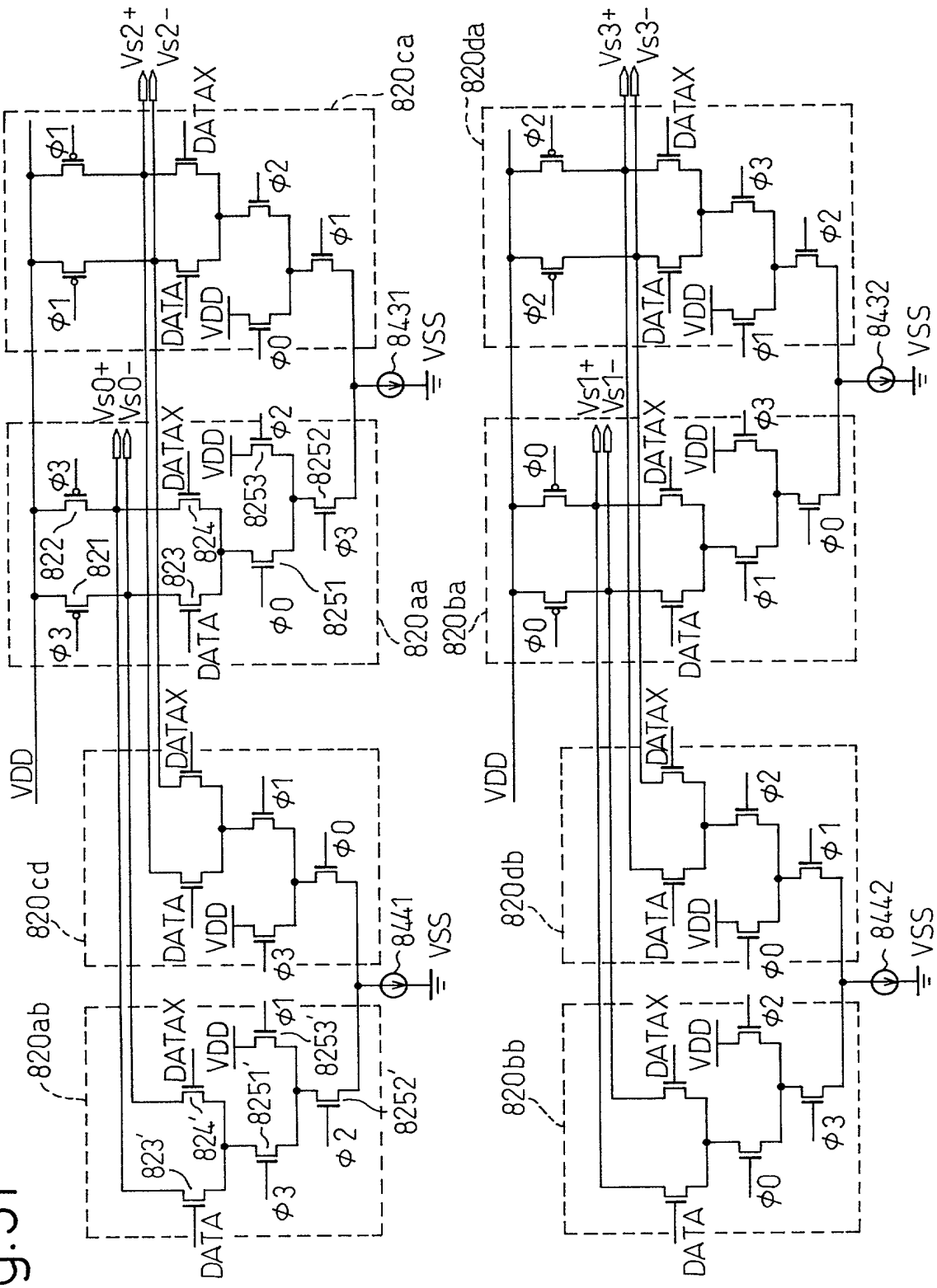
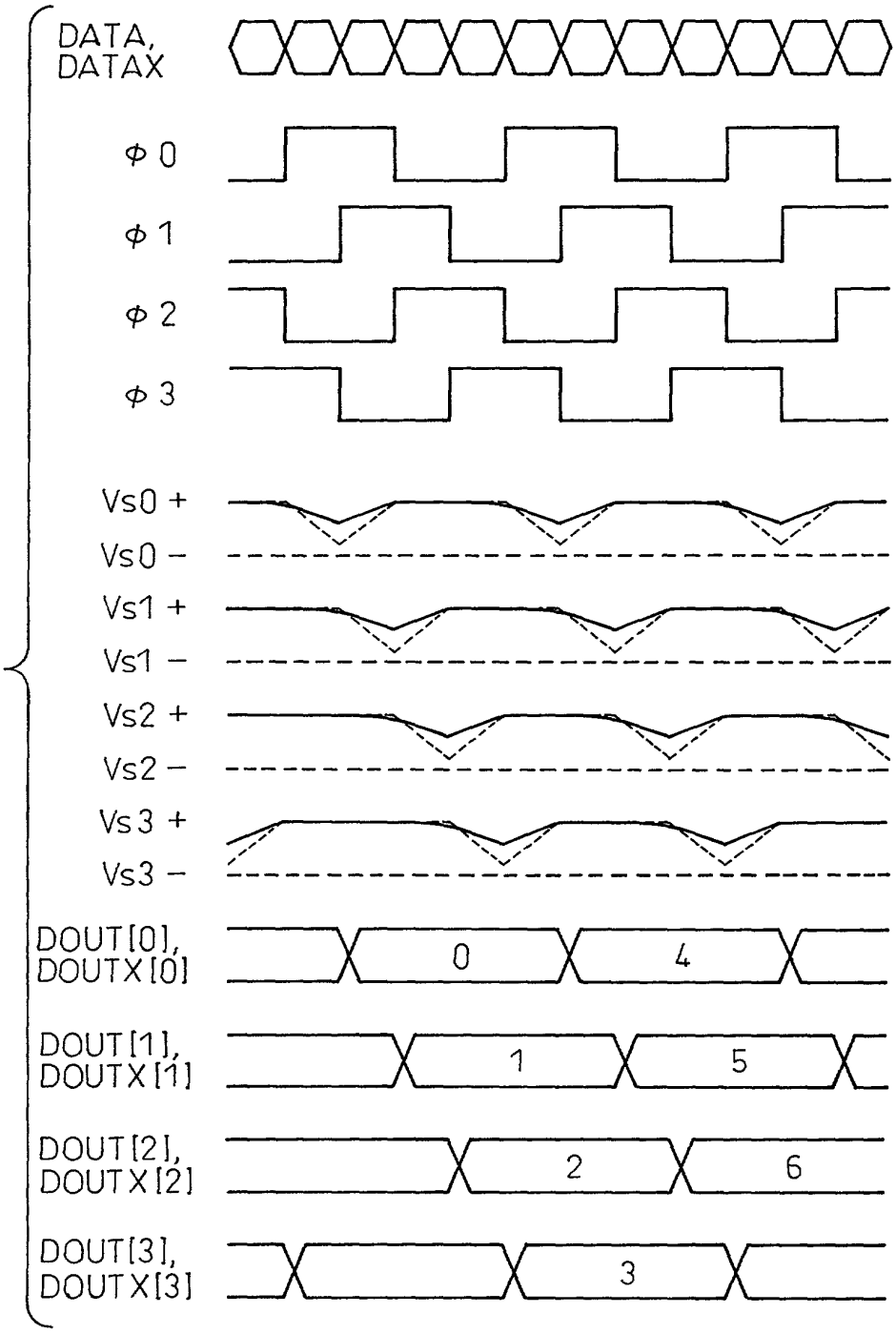

820ca
820da
820aa
820ba
820cd
820db
820ab
820bb
Vs2+
Vs2-
Vs3+
Vs3-
Vs0+
Vs0-
Vs1+
Vs1-
VDD
VSS
DATA
DATAX
8431
8432
8441
8442
8251
8252
8253
8251'
8252'
8253'
821
822
823
824
823'
824'
φ0
φ1
φ2
φ3

Fig.32


DATA,
DATAX
Φ0
Φ1
Φ2
Φ3
Vs0 +
Vs0 −
Vs1 +
Vs1 −
Vs2 +
Vs2 −
Vs3 +
Vs3 −
DOUT[0],
DOUTX[0]
0
4
DOUT[1],
DOUTX[1]
1
5
DOUT[2],
DOUTX[2]
2
6
DOUT[3],
DOUTX[3]
3